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INITIALS

041994

CONTENTS

Entered or Counted			Received or Mailed
	1.	Application ✓ papers. + prints	
11/30	2.	rej (3 mo)	12/7/87 NR
	3.	Amendt A & ext of time	4-11-88
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35 U.S.C. 11/17/88

SERIAL NUMBER (Series of 1987)	PATENT DATE	PATENT NUMBER
041994	MAR 07 1989	

SERIAL NUMBER	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	EXAMINER
07/041,994	04/24/87	357	46	253	JACKSON

APPLICANTS

KLAS H. EKLUND, LOS GATOS, CA.

CONTINUING DATA********

VERIFIED

---JJ--- none

FOREIGN/PCT APPLICATIONS********

VERIFIED

---JJ--- none

FOREIGN FILING LICENSE GRANTED 05/27/87 ***** SMALL ENTITY *****

Foreign priority claimed 35 USC 119 conditions met / Verified and Acknowledged Examiner's Initials	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
☐ yes ☒ no / ☐ yes ☒ no		CA	2	18	3	$ 170.00	SS-520-01

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TITLE

HIGH VOLTAGE MOS TRANSISTORS

U.S. DEPT. of COMM.-Pat. & TM Office — PTO-436L (rev. 10-78)

PARTS OF APPLICATION FILED SEPARATELY SN

NOTICE OF ALLOWANCE MAILED	PREPARED FOR ISSUE	CLAIMS ALLOWED
8-25-88	8/24/88 Jerome Jackson Assistant Examiner	Total Claims: 7 / Print Claim: 1

ISSUE FEE		DRAWING		
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.	Print Fig.
280-	10/24/88	2	5	1

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253 Primary Examiner

ISSUE CLASSIFICATION		ISSUE BATCH NUMBER
Class	Subclass	
357	46	L66

Label Area

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Form PTO-436 (Rev. 9/86)

T NUMBER

APPLICATION SERIAL NUMBER
041994

APPLICANT'S NAME (PLEASE PRINT)
Eklund

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION (INT. CL. 4)

H	01	L		27/02
H	01	L		29/78
H	01	L		29/80
				/

ORIGINAL CLASSIFICATION

CLASS	SUBCLASS
357	46

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
357	22	234	238	

GROUP ART UNIT
253

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
Jerome Jackson Jr.

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
ANDREW J. JAMES

PTO 270 (10-84)

ISSUE CLASSIFICATION SUPERVISORY PAT: . U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE
GROUP ART UNIT 253

FORM PTO-875 (REV. 1-86) — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

PATENT APPLICATION FEE DETERMINATION RECORD

SERIAL NO. 041994 | FILING DATE April 24, 1987

APPLICANT (FIRST NAMED) Klas H. Eklund

CLAIMS AS FILED - PART I

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	18 -20-	* 0
INDEP. CLAIMS	3 -3-	* 0
☐ MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in col. 1 is less than zero, enter "0" in col. 2

SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
	$170	OR		$340
X6=	$	OR	X12=	$
X17=	$	OR	X34=	$
X58=	$	OR	X110=	$
TOTAL	$170	OR	TOTAL	$

CLAIMS AS AMENDED - PART II

	(1)		(2)	(3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
TOTAL	* 7	MINUS	** 20	-
INDEP.	* 2	MINUS	*** 3	-
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADDIT. FEE
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+50=	$		+100=	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

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AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
TOTAL	* 7	MINUS	** 20	—
INDEP.	* 2	MINUS	*** 3	—
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADDIT. FEE
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X5=	$		X10=	$
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+50=	$		+100=	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

	(1)		(2)	(3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
TOTAL	*	MINUS	**	-
INDEP.	*	MINUS	***	-
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

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X15=	$		X30=	$
+50=	$		+100=	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.

** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest No. Previously Paid For" (Total or Indep.) is the highest number found in the appropriate box in Col. 1.

PTO-1130 (Rev. 3-83) 041994

PALM III APPLICATION FILE DATA CODING SHEET

U.S. DEPARTMENT OF COMMERCE—PATENT & TM OFFICE

PREPARED BY: [illegible] DATE: 5/22/97

FORMAT NO. 2 Serial No.	TYPE APPL	FILING DATE Month	Day	Year	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWINGS	ASGT?	TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE RECEIVED	SECURITY CASE?	FOREIGN LICENSE?
08	1	04	24	87		253	351	02	N	018	003	1	0170	N	N

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Atty.'s Reg. Nos. — ☑ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 4 Applicant's Name & Address — ☑ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 5 Title of Invention — ☑ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 6&7 Correspondence Address — ☑ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 8

		CONTINUITY CODE	PARENT APPLICATION SERIAL NUMBER	PARENT FILING DATE Month Day Year	STATUS CODE	PARENT PATENT NUMBER
RECORD	801		0			
RECORD	802		0			
RECORD	803		0			
RECORD	804		0			
RECORD	805		0			
RECORD	806		0			
RECORD	807		0			
RECORD	808		0			
RECORD	809		0			
☐ MORE ON SUPPLEMENTAL CODING SHEET RECORD	810		0			

FORMAT NO. 9

FOREIGN PRIORITY CLAIMED? ☐ YES ☑ NO

☐ APPLICATION PAPERS

		COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FILING DATE Month Day Year
RECORD	901			
RECORD	902			
RECORD	903			
RECORD	904			
RECORD	905			
RECORD	906			
RECORD	907			
RECORD	908			
RECORD	909			
☐ MORE ON SUPPLEMENTAL CODING SHEET RECORD	910			

[redacted]

SEARCHED

Class	Sub.	Date	Exmr.
357	23.8 23.4 46	7/87	JJ
update		8/88	JJ
357	22		

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
357	23.4 23.8 46 22	8/88	JJ

SEARCH NOTES

	Date	Exmr.

[redacted]

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INDEX OF CLAIMS

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Claim Final	Claim Original	Date
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SYMBOLS

√ ..... Rejected
= ..... Allowed
- (Through numeral) Canceled
+ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

PATENT APPLICATION SERIAL NO. 041994

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

050 04/30/87 041994 1 201 170.00 CK

170.00 201 a

41994 PATENT

Case Docket No. SS-520-01

Date April 20, 1987

THE COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor: Klas H. Eklund

For: HIGH VOLTAGE MOS TRANSISTORS

Enclosed are:

11 Pages of specification 1 Pages of abstract 5 Pages of claims

2 Sheets of drawing ____ formal x informal

____ An assignment of the invention to _____

_____

____ A certified copy application(s) _____

_____ from which priority is claimed.

CLAIMS AS FILED				
	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE $340.00
Total Claims	18 -20 =	0	x $12.00	0
Independent Claims	3 -3 =	0	x $34.00	0
Multiple Dependent Claims, if any			$110.00	0

Filing Fee $ 340.00

[X] A verified statement that this is a filing by a small entity is attached. The fee due is fifty percentum of the above.

Filing Fee $ 170.00

[X] The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

[X] A check in the amount of $170.00; ____ This includes $7.00 for recording the assignment.

Attorney for Applicant Reg. No.: 22,611

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, CA 95054
(408) 727-7077

041,994

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

To the Commissioner of Patents and Trademarks:

Your petitioner, KLAS H. EKLUND, a citizen of Finland and resident of Los Gatos, California, whose post office address is 243 Mistletoe Road, 95030, prays that letters patent may be granted to him for

501

HIGH VOLTAGE MOS TRANSISTORS

set forth in the following specification.

041994

High Voltage MOS Transistors

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance,

the net number of charges should be around $1x10^{12}/cm^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on}xA$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on}xA$ is typically 10 - 15 $\Omega\,mm^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 $\Omega\,mm^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, R_{on} x A, of about 2.0 $\Omega\,mm^2$,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0\ \Omega\ mm^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

Fig. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

Fig. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

Fig. 3 is a diagrammatic view of the transistors shown in Figs. 1 and 2 forming a complementary pair on the same chip.

Fig. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in Fig. 3.

Fig. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at Fig. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p^+ material and a pocket 21 of n^+ material are diffused into the p^- substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n^+ material is diffused into the substrate. An

extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1 \times 10^{12}/cm^2$ to around $2 \times 10^{12}/cm^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off

voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of $5 \times 10^{16} - 1 \times 10^{17}/cm^3$. At doping levels above $10^{16}/cm^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1 \times 10^{12}/cm^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0\ \Omega\,mm^2$ for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about $10 - 15\ \Omega\,mm^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of $3 - 4\ \Omega\,mm^2$.

With reference to Fig. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n^+ type material and a pocket 36 of p^+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from beneath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p^+ drain contact pocket 38 and the n-well.

Looking now at Fig. 3, an n-channel transistor 10, similar to that shown in Fig. 1, and a p-channel transistor 30, similar to that shown in Fig. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to Figs. 1 and 2, no further description is considered necessary.

As shown in Fig. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in Fig. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p^+ pocket 49 and an n^+ pocket 51 are provided in the p^- substrate beneath the source contact. The n^+ pocket extends to beneath the gate. An n^+ pocket 52 is provided

beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n^+ pocket 58 and a p^+ pocket 59 are provided in the n-well beneath the source contact and a p^+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

Fig. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n^+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dixode layer thereabove. Beneath the drain contact is an n^+ type pocket 74 and an n-type extended drain region 76. A top layer ~~72~~ 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the

punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about 2.0 Ωmm^2. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all

alterations and modifications as fall within the true spirit and scope of the invention.

12 Cm I claim:

IN THE CLAIMS

1. A high-voltage MOS transistor comprising an insulated-gate field-effect transistor, and a double-sided junction-gate field-effect transistor connected in series, said transistors being united in one structure.

2. In a high-voltage MOS transistor having a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated-gate device and the drain, said extended drain region being formed on material having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

3. A high-voltage MOS transistor comprising a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated gate device and the drain, said extended drain region being formed on material having a

conductivity-type opposite that of the extended drain region, and a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

4. The high-voltage MOS transistor of claim 1 further including,

another high-voltage MOS transistor of opposite conductivity-type forming a complementary pair on the same chip.

5. The high-voltage MOS transistor of claim 2 wherein,

said layer on top of the extended drain region is an ion-implantation.

a

~~6.~~ 2 The high-voltage MOS transistor of claim ~~5~~ 4' wherein,

said top layer has a depth of one-micron or less.

a

~~7.~~ 3 The high-voltage MOS transistor of claim ~~5~~ 4' wherein,

said top layer has a doping density higher than 5 x $10^{16}/cm^3$ so that the mobility starts to degrade.

8. The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of n-type conductive material and said top layer is made of p-type conductive material.

9. The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of p-type conductive material and said top layer is made of n-type conductive material.

10. The high-voltage MOS transistor of claim 9 wherein,

said transistor is embedded in a well of n-type conductive material in a substrate of p-type conductive material, and further including a complementary high-voltage MOS transistor having an extended drain of n-type conductive material embedded in the substrate.

11. The high-voltage MOS transistor of claim 3 wherein,

both the extended drain region and the top layer of material are diffusions or ion implantations into a substrate or epitaxial layer.

12. The high-voltage MOS transistor of claim 11 wherein,

said extended drain region and the top layer of material are formed by using the same mask (self alignment).

13. The high-voltage MOS transistor of claim 3 wherein,

the material on which the extended drain region is formed is a substrate; and

the substrate is of one conductivity-type material, and further including a complementary transistor embedded in a well or epi-island of opposite conductivity-type material on the same substrate.

14. The complementary pair of high-voltage MOS transistors of claim 13 wherein,

the well in which the complementary transistor is embedded is the same diffusion as the extended drain for the other transistor.

15. The complementary pair of high-voltage MOS transistors of claim 14 wherein,

the well is an n-well and further used for a low voltage p-channel device.

16. The high-voltage MOS transistor of claim 2 wherein,

the top layer is floating.

17. The high-voltage MOS transistor of claim 3 wherein,

the source region and the drain region are formed in a similar manner.

18. The high-voltage MOS transistor of claim 3 further including,

low voltage logic and analog function on the same chip.

Add q2

ABSTRACT OF THE DISCLOSURE

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH VOLTAGE MOS TRANSISTORS

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as Application Serial No._____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Thomas E. Schatzel Reg. No. 22,611
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Address all telephone calls to Thomas E. Schatzel at telephone No. (408) 727-7077.

Address all correspondence to:

LAW OFFICES OF THOMAS E. SCHATZEL
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Santa Clara, California 95054-3093

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter to each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: 4/01-dp KLAS H. EKLUND

Inventor's Signature: _____ Date: 4/17/87

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Applicant or Patentee: KLAS H. EKLUND
Serial or Patent No.:
Filed or Issued:
For: HIGH VOLTAGE MOS TRANSISTORS

Attorney's Docket No.: 520-01

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled HIGH VOLTAGE MOS TRANSISTORS described in

[X] the specification filed herewith
[ ] application serial no. _____, filed _____
[ ] patent no. _____, issued _____.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

[X] no such person, concern, or organization
[ ] persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME n/a
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I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
KLAS H. EKLUND		
Signature of Inventor	Signature of Inventor	Signature of Inventor
4/17/87		
Date	Date	Date

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KLAS H. EKLUND

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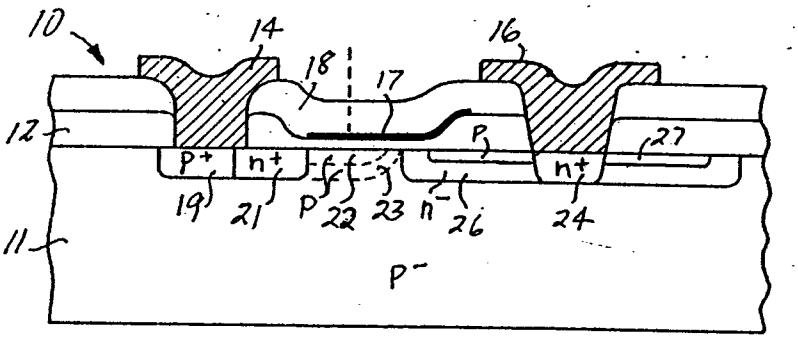

Fig. 1

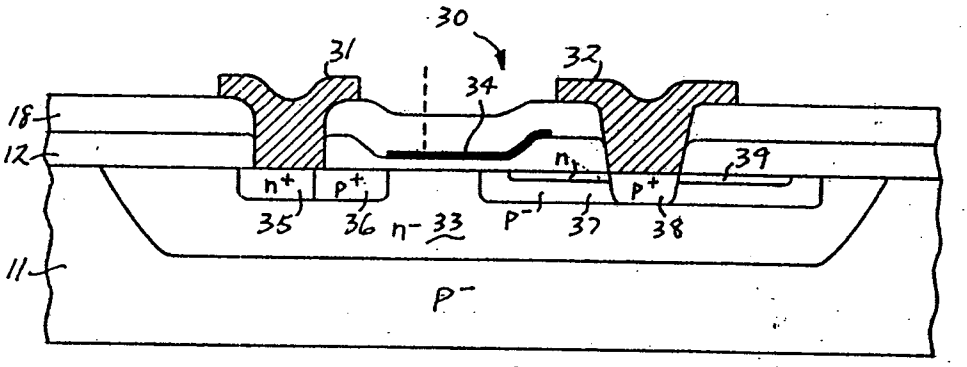

Fig. 2

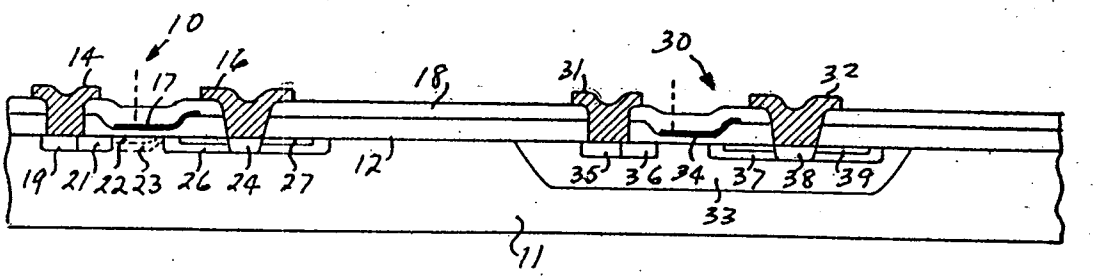

Fig. 3

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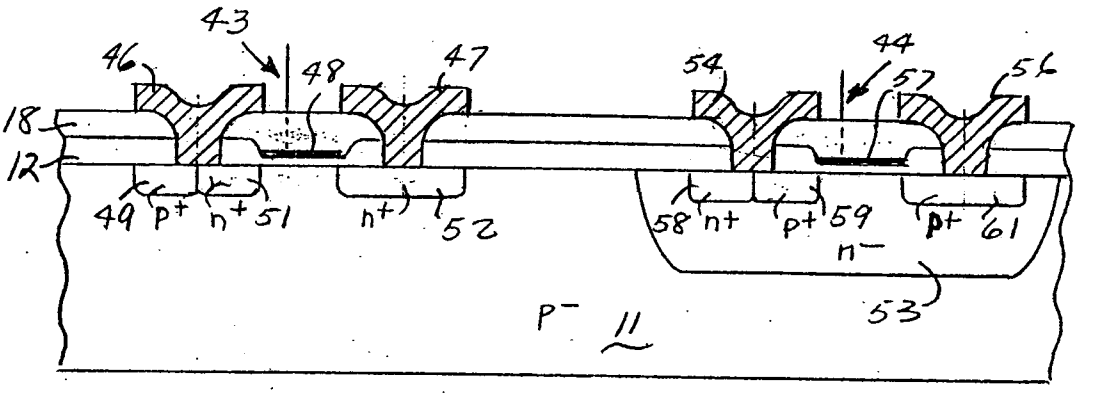

Fig-4

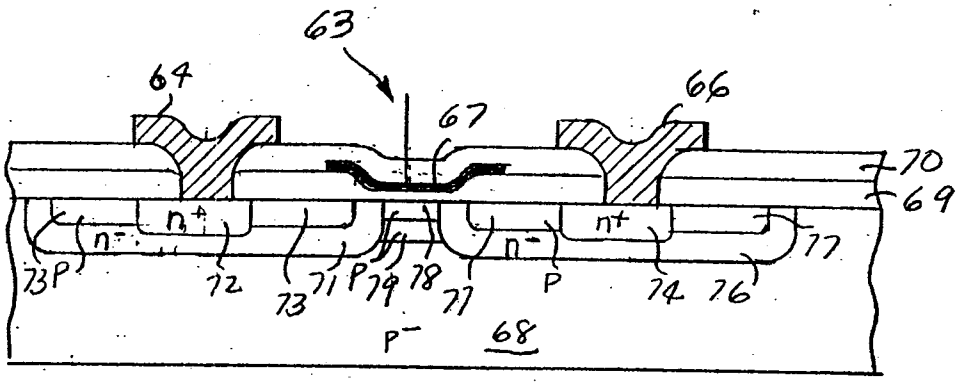

Fig-5

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Conventional NMOS

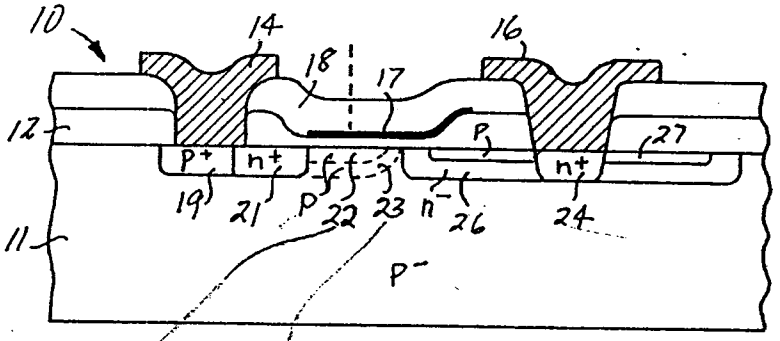

Fig-1

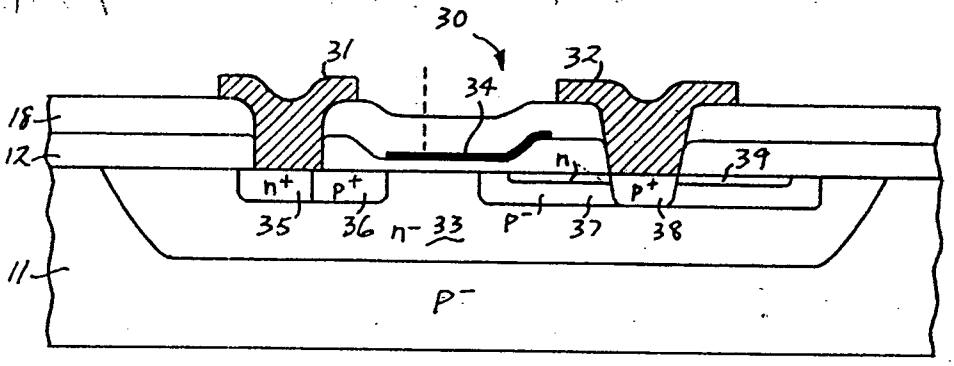

Fig-2

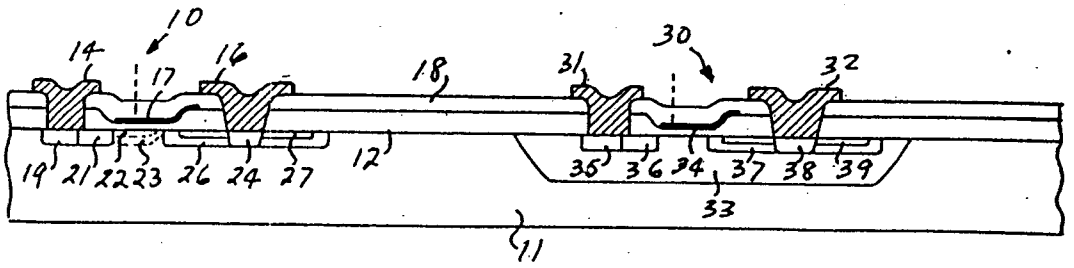

Fig-3